IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a divisional of application Serial No. 09/247,009, filed February 8, 1999, ~~pending~~ now U.S. Patent 6,351,028, issued February 26, 2002.

Please replace paragraph number **[0007]** with the following rewritten paragraph:

[0007] The `745 patent discloses a stacked semiconductor device carrier assembly and a method for packaging interconnecting semiconductor devices. The carriers are constructed from a metal substrate onto which the semiconductor device attaches. Next, the semiconductor device is wired bonded to the conductor pattern on the substrate and each conductor is routed to the edge of the substrate where it is connected to a half circle of a metallized through-hole. Again, the `745 patent discloses a ~~tube like~~ tube-like design with half circle vias for allowing interconnection to the stack of multiple semiconductor devices.

Please replace paragraph number **[0020]** with the following rewritten paragraph:

[0020] FIG. 10 is a block diagram of an electronic system incorporating the semiconductor device of FIG. 2 and the present invention.

Please replace paragraph number **[0022]** with the following rewritten paragraph:

[0022] This protects the semiconductor devices 24 during the stacking and enables a variety of interconnections to be used between semiconductor devices 24, T-interposers 26, and/or substrates 22. The interconnection between semiconductor devices 24 or T-interposers 26 or substrates 22, or both, uses conductor traces, tape, wire bonding, conductive paste, or conductive adhesives, or any other type of suitable semiconductor interconnection technique known to one skilled in the art. The T-interposer 26 allows bond pads 28 of the semiconductor device 24 to be exposed, so no additional rerouting steps are required to reroute a bond pad 28 to the edges. This is advantageous over the prior art structures, such as the cubic design shown in drawing FIG. 1, in that the shell case or the interconnection requires additional processing in

those materials and additional time. Further, the flanged edges forming the stem 27 of T-interposer 26 allow direct connection to the bond pads 28 and contact to all four sides of semiconductor devices 24. This allows increased interconnect density between a substrate and a plurality of semiconductor devices.

Please replace paragraph number **[0024]** with the following rewritten paragraph:

[0024] Referring to drawing FIG. 3, further illustrated is an inverted T-interposer 26 as shown in drawing FIG. 2. Again, T-interposer 26 can be manufactured to match the same CTE of the semiconductor device 24 or the semiconductor device substrate 22 used for each of semiconductor devices 24, or both. This allows T-interposer 26 to serve as a thermal or heat dissipation device between each semiconductor device 24 while allowing for greater heat dissipation than would otherwise be possible were the semiconductor devices 24 stacked directly upon each other. Further, T-interposer 26 provides electrical insulation between each semiconductor device 24 that would not be otherwise possible were the semiconductor devices to be stacked one upon another such as in the prior art described in drawing FIG. 1. Additionally, the T-interposer 26 may be comprised of two different materials to provide both thermal conductivity from one semiconductor device and thermal insulation with respect to a second semiconductor device. For instance, the stem 27 may be of a thermally conductive material while the T-bar members 29 are formed of a thermally insulative material, the stem 27 may be joined to the T-bar member(s) 29 by any suitable means, such as adhesive bonding, etc. The T-interposer 26 of the present invention provides for much greater bonding edge relief for different types of connection devices with respect to the bond pad location on the active surface of the semiconductor device 24 than that shown in the prior art device illustrated in drawing FIG. 1 and greater insulation capacity for the bond pads 28 of the semiconductor devices 24 with the T-interposer 26 in place. Finally, a top T-interposer 26 is further provided for capping the device to protect and promote heat transfer from the last semiconductor device 24 forming the multiple stacked unit 20.

Please replace paragraph number **[0026]** with the following rewritten paragraph:

[0026] Referring to drawing FIG. 4, illustrated is a cross-section diagram of multiple semiconductor devices 38 and 40 being mounted to a single T-interposer 26. T-interposer 26 is mounted to a substrate 36. Substrate 36 includes ~~bonding~~ bond pads/circuits 28 thereon. Semiconductor device 38 can be a processor type semiconductor device while semiconductor device 40 can be a memory type semiconductor device. Semiconductor device 38 and semiconductor device 40 are interconnected via bond pads 28 and further connected to pads or circuits 28 on substrate 36. Additionally, the bonding wire from one pad or circuit 28, such as ~~on die~~ on device 40, can connect directly to the device structure to which the substrate 36 is to be permanently mounted. This can be the actual circuit board, such as a mother board used in a computer system. Of course, other direct connection options will be readily apparent to one skilled in the art.

Please replace paragraph number **[0029]** with the following rewritten paragraph:

[0029] Referring to drawing FIG. 7, illustrated is a cross-sectional view of a multiple stack unit 20 that is completely sealed or packaged. Again, a substrate 22 is provided upon which a first semiconductor device 24 is mounted ~~with an~~ with a T-interposer 26 mounted to the first semiconductor device 24. A final cap or top T-interposer 26 is further provided on top of the entire stack unit 20. Lastly, an epoxy interconnect 50 is provided for sealing and/or packaging and electrically isolating the bonding performed between the multiple semiconductor devices 24. If desired, the top of the unit 20 may include a heat sink 52 of suitable type material which may include one or more fins 54 (shown in dashed lines) for additional thermal control of the heat from the unit 20.

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] Referring to drawing FIG. 8, illustrated is another embodiment of the T-interposer 26 of the present invention in a stacked arrangement between semiconductor devices 40 which are electrically connected by wires 56 to circuits 58 of the substrate 36. In this

embodiment of the T-interposer 26 of the present invention, one T-bar member 29 has a greater length or extends farther than the opposing T-bar member 29 of the T-interposer 26 to provide greater bonding edge relief for different types of connection devices with respect to the bond pad location on the active surface of the semiconductor device 24 than the bonding edge relief provided by the T-bar member 29 on the other side of the T-interposer 26. In this manner, the T-interposer 26 is not centrally located on a portion of the active surface of the semiconductor device 40 but, rather, is located off-center on a portion of the active surface of the semiconductor device 40. Such a T-interposer 26 allows for the accommodation of differing sizes and shapes of semiconductor devices 40 and bond pad arrangements thereon for interconnection to the circuits 58 of substrate 36.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] Referring to drawing FIG. 9, illustrated is another embodiment of the T-interposer 26 of the present invention where the T-interposer 26 includes a plurality of stems 27 and T-bar members 29 to form the same, each stem 27 located on a portion of the active surface of a semiconductor device 40 which is, in turn, located on a substrate 36 having circuits 58 located thereon connected by wires 56 while wires 62 electrically connect the semiconductor devices 40 located on surface 29′ of the T-interposer 26 to the circuits 60 located thereon. In this manner, the T-interposer 26 helps to increase the density of the semiconductor devices 40 located on the substrate 36 while providing thermal control of the heat generated from the semiconductor devices 40 located on the substrate 36 and on the surface 29′ of the T-interposer 26.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] As shown in drawing FIG. 10, an electronic system 130 includes an input device 132 and an output device 134 coupled to a processor device 136 which, in turn, is coupled to a memory device 138 incorporating the exemplary ~~integrated circuit die~~ semiconductor device 24 and T-interposer 26 of drawing FIG. 2.

IN THE CLAIMS:

Claims 2, 4, 10 and 12 have been amended herein. All of the pending claims 1 through 16 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Previously presented) A method of forming a multiple semiconductor device stack apparatus comprising:

providing a substrate;

providing a first semiconductor device having at least one bond pad on an active surface thereof;

mounting and electrically connecting said first semiconductor device to said substrate;

providing a first interposer device;

mounting said first interposer device to said first semiconductor device, on a side opposite said substrate, said first interposer device having a first surface of a first area and a second surface of a second area less than said first area with a first pair of recesses formed on opposing edges of said first interposer device thus exposing said at least one bond pad on said active surface of said first semiconductor device, said second surface mounted to said active surface of said first semiconductor device;

providing a second semiconductor device; and

mounting said second semiconductor device on said first surface of said first interposer device, opposite said first semiconductor device and electrically connecting said second semiconductor device to either said first semiconductor device or to said substrate or both.

2. (Currently amended) The method of forming a multiple semiconductor device stack apparatus according to claim 1, further comprising:

providing a second interposer device having a first side and a second side; and

mounting said second interposer device to said second semiconductor device on said first side,

wherein said second interposer device includes a bond pad recess opening for allowing connection between either said first and second semiconductor devices or between said first and second semiconductor devices and said substrate or both.

3. (Previously presented) A method of forming a multiple semiconductor device stack apparatus comprising:

providing a substrate;

providing a first semiconductor device having at least one bond pad on an active surface thereof;

mounting and electrically connecting said first semiconductor device to said substrate;

providing a first thermally conductive interposer device;

mounting said first thermally conductive interposer device to said first semiconductor device, on a side opposite said substrate, said first thermally conductive interposer device having a first surface of a first area and a second surface of a second area less than said first area with a first pair of recesses formed on opposing edges of said first thermally conductive interposer device thus exposing said at least one bond pad on said active surface of said first semiconductor device, said second surface mounted to said active surface of said first semiconductor device;

providing a second semiconductor device; and

mounting said second semiconductor device on said first surface of said first thermally conductive interposer device, opposite said first semiconductor device and electrically connecting said second semiconductor device to either said first semiconductor device or to said substrate or both.

4. (Currently amended) The method of claim 3, further comprising:
providing a second interposer device having a first side and a second side; and
mounting said second interposer device to said second semiconductor device on said first side thereof, wherein said second interposer device includes a bond pad recess opening for allowing connection between either said first and second semiconductor devices or between said first and second semiconductor devices and said substrate or both.

5. (Original) The method of claim 4, wherein said second interposer device comprises a thermally conductive interposer.

6. (Original) The method of claim 4, wherein said second interposer device comprises a thermally insulative interposer.

7. (Original) The method of claim 4, wherein said second interposer device comprises a thermally conductive and thermally insulative interposer.

8. (Original) The method of claim 3, wherein said first thermally conductive interposer device includes a thermally insulative portion.

9. (Previously presented) A method for forming a stack of multiple semiconductor devices comprising:
providing a substrate;
providing a first semiconductor device having at least one bond pad on an active surface thereof;
mounting and electrically connecting said first semiconductor device to said substrate;
providing a first interposer device;
mounting said first interposer device to said first semiconductor device, on a side opposite said substrate, said first interposer device having a first surface of a first area and a second surface of second area less than said first area with a first pair of recesses formed on

opposing edges of said first interposer device thus exposing said at least one bond pad on said active surface of said first semiconductor device, said second surface mounted to said active surface of said first semiconductor device;

providing a second semiconductor device; and

mounting said second semiconductor device on said first surface of said first interposer device, opposite said first semiconductor device and electrically connecting said second semiconductor device to either said first semiconductor device or to said substrate or both.

10. (Currently amended) The method of claim 9, further comprising:

providing a second interposer device having a first side and a second side; and

mounting said second interposer device to said second semiconductor device on said first side, wherein said second interposer device includes a bond pad recess opening for allowing connection between either said first and second semiconductor devices or between said first and second semiconductor devices and said substrate or both.

11. (Original) A method of forming a stack of semiconductor devices comprising:

providing a substrate;

providing a first semiconductor device having at least one bond pad on an active surface thereof;

mounting and electrically connecting said first semiconductor device to said substrate;

providing a first thermally conductive interposer device;

mounting said first thermally conductive interposer device to said first semiconductor device, on a side opposite said substrate, said first thermally conductive interposer having a first surface of a first area and a second surface of a second area less than said first area with a first pair of recesses formed on opposing edges of said first thermally conductive interposer device thus exposing said at least one bond pad on said active surface of said first semiconductor device, said second surface mounted to said active surface of said first semiconductor device;

providing a second semiconductor device; and

mounting said second semiconductor device on said first surface of said first thermally conductive interposer device, opposite said first semiconductor device and electrically connecting said second semiconductor device to either said first semiconductor device or to said substrate or both.

12. (Currently amended) The method of claim 11, further comprising:

providing a second interposer device having a first side and a second side; and

mounting said second interposer device to said second semiconductor device on said first side thereof, wherein said second interposer device includes a bond pad recess opening for allowing connection between either said first and second semiconductor devices or between said first and second semiconductor devices and said substrate or both.

13. (Original) The method of claim 12, wherein said second interposer device comprises a thermally conductive interposer.

14. (Previously presented) The method of claim 12, wherein said second interposer device comprises a thermally insulative interposer.

15. (Previously presented) The method of claim 12, wherein said second interposer device comprises a thermally conductive and thermally insulative interposer.

16. (Original) The method of claim 11, wherein said first thermally conductive interposer device includes a thermally insulative portion.

REMARKS

Please note that the Notice of Allowability, Form PTO-37, indicates that the allowed claims are 1 through 15; however, applicant respectfully submits that the allowed claims are actually claims 1 through 16.

This amendment corrects errors in the text and drawings. Entry is respectfully solicited.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,

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Date: October 6, 2003
JRD/csw:jml

Enclosures: Replacement Sheets
Annotated Sheets Showing Changes

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IN THE DRAWINGS:

The attached sheets of drawings include changes to FIGS. 1 and 10. These sheets, which include FIGS. 1-3 and 10, replace the original sheets including FIGS. 1-3 and 10.

Specifically, FIG. 1 has been revised to change the reference numeral "5" to --2--; and FIG. 10 has been revised to change the reference numeral "12" to --24, 26--. No new matter has been added.

AMENDMENTS TO THE ABSTRACT:

Please replace the Abstract originally appearing on page 17 of the application with the following rewritten paragraph:

ABSTRACT OF THE DISCLOSURE

Multiple integrated circuit devices in a stacked configuration that ~~uses a~~ use a spacing element for allowing increased device density and increased thermal conduction or heat removal for semiconductor devices and the methods for the stacking thereof are disclosed.

0001/5

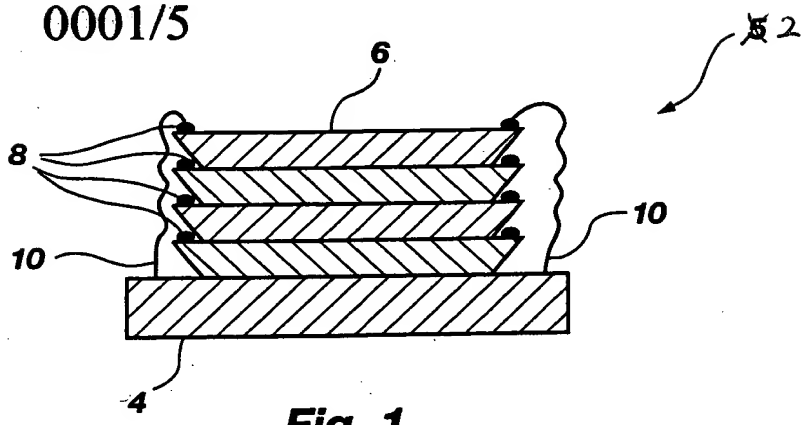

Fig. 1
(PRIOR ART)

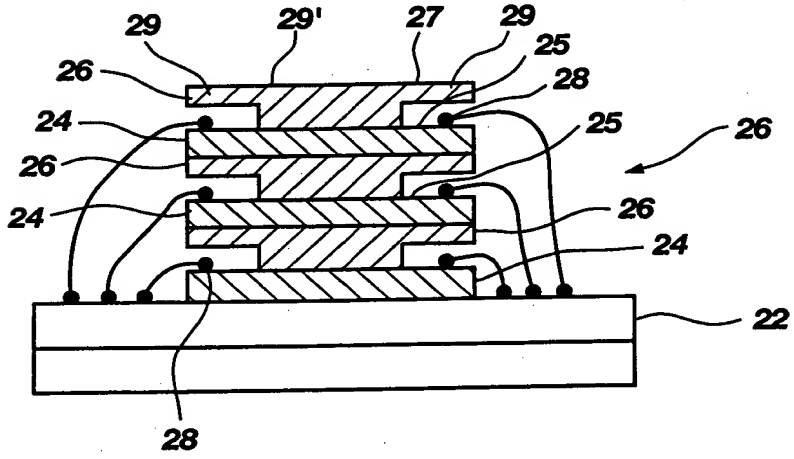

Fig. 2

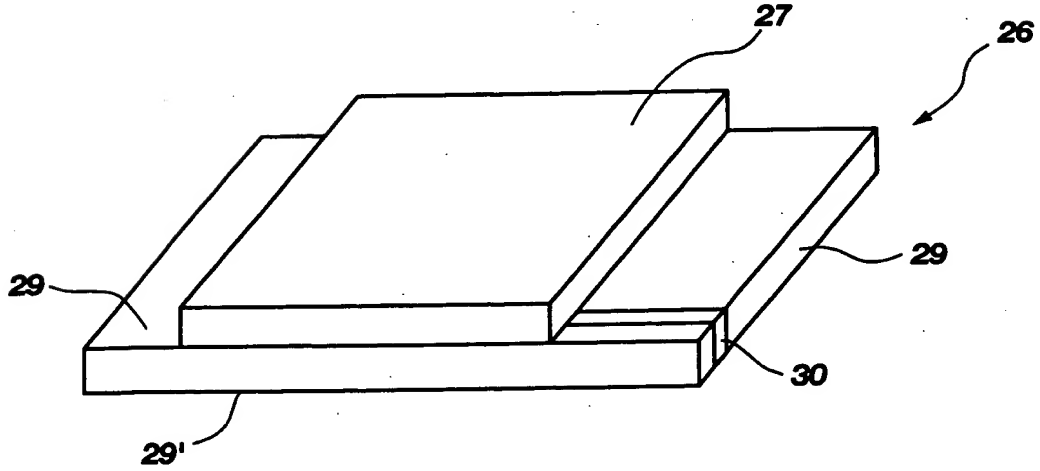

Fig. 3

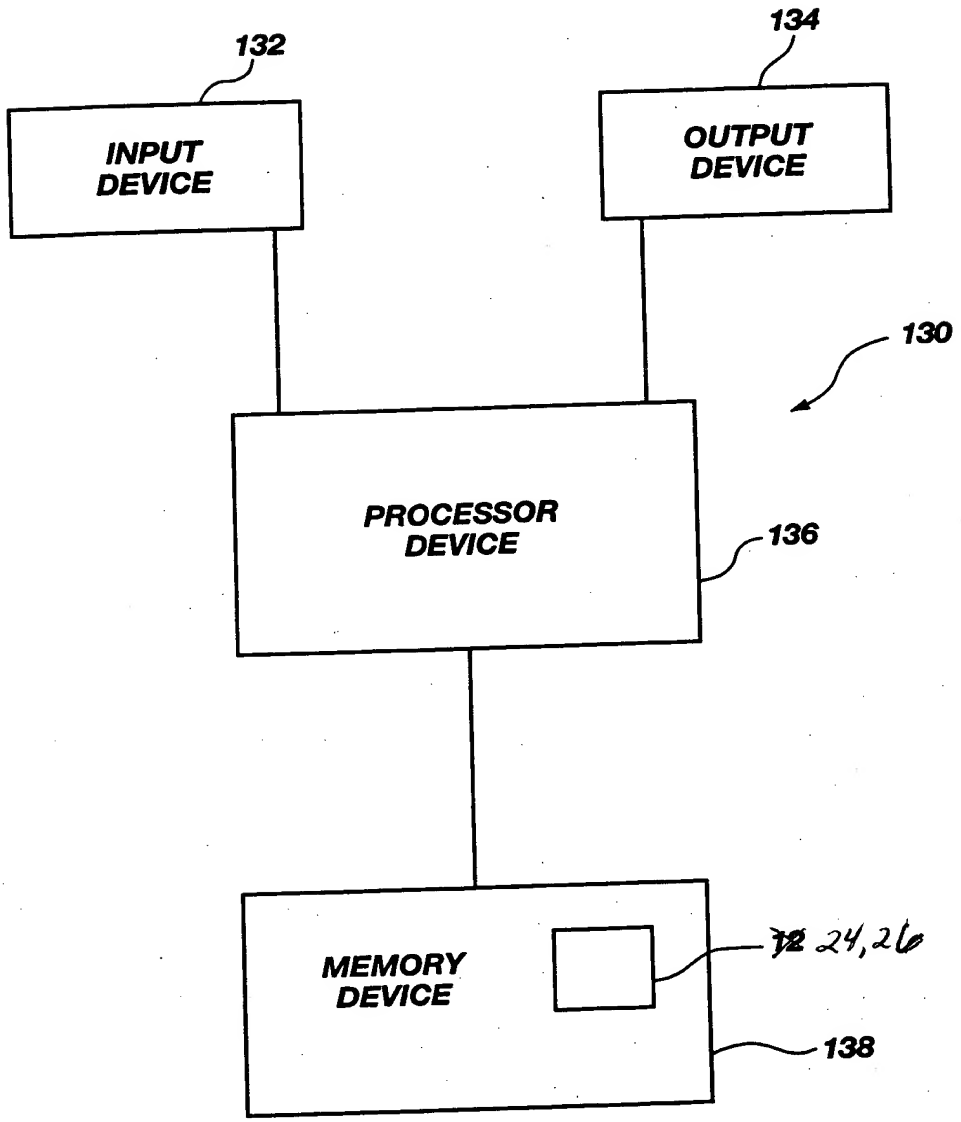

Fig. 10